REMARKS

The above amendments and these remarks are responsive to the Office Action issued on June 3, 2004. By this response, claims 1, 3, 4, 7, 10-13 and 15 are amended, and claim 14 is cancelled without prejudice. The specification is also amended to use terms consistent to the claims. No new matter is added. Claims 1-13 and 15-19 are now active for examination.

The Office Action

The Office Action dated June 3, 2004 rejected claims 1-9 and 14-18 under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement, and claims 1-9 and 10-19 under 35 U.S.C. §112, second paragraph as being indefinite. Claims 10-13 were rejected under 35 U.S.C. §102(b) as being anticipated by Okado (EP 0 511 484 A2). Claims 1-9 and 14-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Okado in view of Hennessy. The Office Action rejected claim 19 under 35 U.S.C. §103(a) as being unpatentable over Okado in view of Watanabe (5,214,786). The Examiner objected to claims 10-13 for including unclear claim language.

It is respectfully submitted that in view of the amendments and remarks presented herein, the objection is addressed and the claim rejections are overcome.

The Rejection of Claim 14 Is Now Moot

By this Response, claim 14 is cancelled without prejudice. Therefore, the rejection of claim 14 is now moot.

The Objection to Claims 10-13 Is Addressed

The Office Action objected to claims 10-13 for including unclear claim limitations. Specifically, the Office Action asserted that the meaning of the description "said memory operation unit generating a pipeline stage corresponding to selection of an instruction memory bank and a pipeline stage corresponding to instruction readout to carry out pipeline processing when a plurality of instructions are fetched from a plurality of said instruction memory banks" in claim 10 is unclear. Claims 11-13 were objected to for their dependencies on claim 10 or for including similar claim language.

By this response, the limitation in claim 10 is amended to read as "said memory operation unit retaining an instruction in a loop of instructions corresponding to a repeat instruction in a dedicated register in said register file when said repeat instruction is executed, and executing the loop of instructions while fetching the instruction retained in said dedicated register." Claims 12 and 13 also are amended to clarify claim scope and to correct clerical errors. It is believed that the scope of claims 10-13 is now clear.

The Rejections Under 35 U.S.C. §112 Are Overcome

Claims 1-9 and 14-18 were rejected as being both indefinite and failing to comply with the enabling requirement. Specifically, the Examiner asserted that it is unclear whether the term "a pipeline stage" used in the claims is a piece of hardware or a processing cycle. The Examiner suggested amending the term "a pipeline stage" to "a pipeline cycle."

By this Response, the claims are amended to replace the term "a pipeline stage" with the term "a pipeline cycle," as suggested by the Examiner. It is believed that the claims 1-9 and 14-18 are now in proper form. Favorable reconsideration of the claims is respectfully requested.

Claim 10 was rejected for failing to provide sufficient antecedent basis for the term "said dedicated register." By this Response, claim 10 is amended to provide appropriate antecedent basis for "said dedicated register." It is respectfully submitted that the rejection of claim 10 under 35 U.S.C. §112, second paragraph is overcome.

The Anticipation Rejection Based on Okado Is Traversed

Claims 10-13 were rejected under 35 U.S.C. §102(b) as being anticipated by Okado. By this Response, independent claim 13 is amended to include substantial descriptions from claim 14. It is respectfully submitted that Okado cannot support a prima facie case of anticipation because Okado fails to teach every limitation of claim 10 after the claim amendment.

Claim 10, as amended, recites:

A data processing apparatus comprising:
...
a register file;
a memory operation unit...fetching an instruction..., and accessing said data memory according to a decoded result of said instruction decoder; and
...
said memory operation unit retaining an instruction in a loop of instructions corresponding to a repeat instruction in a dedicated register in said register file when said repeat instruction is executed, and executing the loop of instructions while fetching the instruction retained in said dedicated register;
wherein said memory operation unit generates a pipeline cycle corresponding to selection of an instruction memory bank and a pipeline cycle corresponding to instruction readout from said selected instruction memory bank to carry out a pipeline process when fetching an instruction from said plurality of instruction memory banks.

Therefore, in an apparatus of claim 10, the memory operation unit generates a pipeline cycle corresponding to selection of an instruction memory bank. In other words, an instruction is read out after selection of an instruction memory bank.

In contrast, Okado merely discusses that a repeat controller 207 causes the instruction registers IR1 and IR2 to retain their instructions depending on the occurrence of an internal state requiring particular instructions held in the micro ROM 201 to be executed repeatedly. In doing

so, the repeat controller 207 controls the timing generator TG and program counter PC to inhibit access to the micro ROM 201 so that the target instructions for recurrent execution will be output repeatedly from instruction registers IR1 and IR2. See column 9, lines 35-45 of Okado. However, Okado does not each that "said memory operation unit generates a pipeline cycle corresponding to selection of an instruction memory bank and a pipeline cycle corresponding to instruction readout from said selected instruction memory bank to carry out a pipeline process when fetching an instruction from said plurality of instruction memory banks," as recited in claim 10. Since Okado fails to teach every limitation of claim 10, Okado cannot support a prima facie case of anticipation. The anticipation rejection of claim 10 based on Okado is untenable and should be withdrawn. Favorable reconsideration of claim 10 is respectfully requested.

Claims 11-13, directly or indirectly, depend on claim 10 and incorporate every limitation thereof. Therefore, the anticipation rejection of claims 11-13 based on Okado also is untenable and should be withdrawn based on at least the same reasons for claim 10 as well as on their own merits. Favorable reconsideration of claims 11-13 is respectfully requested.

The Obviousness Rejection Based on Okado and Hennessy Is Traversed

Claims 1-9 and 15-18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Okado in view of Hennessy. The obviousness rejection of claims 1-9 and 15-18 is respectfully traversed because Okado and Hennessy cannot support a prima facie case of obviousness.

Claim 1, as amended, recites:

> A data processing apparatus comprising:
> an instruction memory...;
> a data memory...
> a memory operation unit connected to said instruction memory, said data memory and said instruction decoder, fetching an instruction stored in said instruction memory, and accessing said data memory according to a decode result of said instruction decoder; and
> ...
> said instruction memory including a plurality of instruction memory banks,

said memory operation unit generating a pipeline cycle corresponding to selection of an instruction memory bank and a pipeline cycle corresponding to instruction readout from said selected instruction memory bank to carry out pipeline processing when a plurality of instructions are fetched from the plurality of instruction memory banks.

Therefore, in an apparatus of claim 1, the memory operation unit generates a pipeline cycle corresponding to selection of an instruction memory bank. In other words, an instruction is read out after selection of an instruction memory bank.

As discussed above, Okado does not each that the memory operation unit generates a pipeline cycle corresponding to selection of an instruction memory bank and a pipeline cycle corresponding to instruction readout from said selected instruction memory bank to carry out a pipeline process when fetching an instruction from a plurality of instruction memory banks, as describes in claim 1. The other reference, Hennessy, does not alleviate the deficiency of Okado. Hennessy merely describes that after a time equal to the memory access time, all the memory banks will have fetched a double precision word, and the words can begin returning to the vector registers. The words are sent serially from the banks, starting with the bank fetching from the lowest address. In other words, according to Hennessy, a bank is selected after an instruction is fetched. Therefore, Hennessy also fails to disclose that "said memory operation unit generating a pipeline cycle corresponding to selection of an instruction memory bank and a pipeline cycle corresponding to instruction readout from said selected instruction memory bank to carry out pipeline processing when a plurality of instructions are fetched from the plurality of instruction memory banks," as recited in claim 1. Thus, Okado and Hennessy, even combined, do not teach every limitation of claim 1. Okado and Hennessy cannot support a prima facie case of obviousness. Accordingly, the obviousness rejection is untenable and should be withdrawn. Favorable reconsideration of claim 1 is respectfully requested.

Claim 2-9, directly or indirectly, depend on claim 1 and incorporate every limitation thereof. Accordingly, the obviousness rejection of claims 2-9 based on Okado and Hennessy also is untenable and should be withdrawn for at least the same reasons as for claim 1, as well as based on their own merits. Favorable reconsideration of claims 2-9 is respectfully requested.

Claims 15-18, directly or indirectly, depend on claim 10, and incorporate every limitation thereof. As discussed earlier, claim 10, as amended, recites "said memory operation unit generates a pipeline cycle corresponding to selection of an instruction memory bank and a pipeline cycle corresponding to instruction readout from said selected instruction memory bank to carry out a pipeline process when fetching an instruction from said plurality of instruction memory banks." In other words, an instruction is read out after selection of an instruction memory bank. As already discussed, neither Okado nor Hennessy teaches or suggests this limitation. Therefore, the obviousness rejection of claims 15-18 based on Okado and Hennessy also is untenable and should be withdrawn for at least the same reasons as for claim 10, as well as based on their own merits. Favorable reconsideration of claims 15-18 is respectfully requested.

The Obviousness Rejection Based on Okado and Watanabe Is Overcome

Claim 19 depends on claim 10 and was rejected as being obvious over Okado in view of Watanabe. As pointed out previously, Okado does not teach that "said memory operation unit generates a pipeline cycle corresponding to selection of an instruction memory bank and a pipeline cycle corresponding to instruction readout from said selected instruction memory bank to carry out a pipeline process when fetching an instruction from said plurality of instruction memory banks," as required by claim 19 by virtue of its dependency from claim 10. Watanabe also fails to teach this feature. Therefore, Okado and Watanabe, even combined, do not teach every limitation of claim 19.

Accordingly, Okado and Watanabe cannot support a prima facie case of obviousness. The obviousness rejection of claim 19 based on Okado and Watanabe is untenable and should be withdrawn. Favorable reconsideration of claim 19 is respectfully requested.

For the reasons given above, Applicants believe that this application is conditioned for allowance and Applicants request that the Examiner give the application favorable consideration and permit it to issue as a patent. However, if the Examiner believes that the application can be put in even better condition for allowance, the Examiner is invited to contact Applicants' representatives listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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BEFORE THE OFFICE OF ENROLLMENT AND DISCIPLINE
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Expires: March 1, 2005

Harry I. Moatz
Director of Enrollment and Discipline